

Single N-Channel MOSFET

■ DESCRIPTION

SMC4234NA is the N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior fast switching performance and withstand high energy pulse in the avalanche and commutation mode.

■ PART NUMBER INFORMATION

SMC 4234 NA - TR G

a	b	c	d	e
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a : Company name.

b : Product Serial number.

c : Package code NA:DFN3.3X3.3A-8

d : Handling code TR:Tape&Reel

e : Green produce code G:RoHS Compliant

■ FEATURES

V_{DS}=20V, I_D=40A

R_{DS(ON)}=2.7mΩ(Typ.)@V_{GS}=10V

R_{DS(ON)}=3.3mΩ(Typ.)@V_{GS}=4.5V

R_{DS(ON)}=4.2mΩ(Typ.)@V_{GS}=2.5V

R_{DS(ON)}=6.6mΩ(Typ.)@V_{GS}=1.8V

◆ 100% EAS Guaranteed

■ APPLICATIONS

◆ Power Management

◆ DC/DC Converters

◆ Battery Powered Systems



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C Unless otherwise noted)

Symbol	Parameter	Rating	Units	
V _{DSS}	Drain-Source Voltage	20	V	
V _{GSS}	Gate-Source Voltage	±12	V	
I _D	Continuous Drain Current (V _{GS} =4.5V)	T _C =25°C	40	A
		T _C =100°C	40	A
I _{DM}	Pulsed Drain Current ^B	120	A	
I _D	Continuous Drain Current (V _{GS} =4.5V)	T _A =25°C	22.6	A
		T _A =70°C	18.1	A
P _D	Power Dissipation ^A	T _A =25°C	4.2	W
		T _A =70°C	2.7	W
I _{AS}	Avalanche Current ^A	35	A	
E _{AS}	Single Pulse Avalanche energy L=0.1mH ^B	61	mJ	
P _D	Power Dissipation ^C	T _C =25°C	29.8	W
		T _C =100°C	11.9	W
T _J	Operation Junction Temperature	-55/150	°C	
T _{STG}	Storage Temperature Range	-55/150	°C	

■ THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
R _{θJA}	Thermal Resistance Junction to Ambient ^A	t≤10s	35	°C/W
	Thermal Resistance Junction to Ambient ^{AC}	Steady-State	65	
R _{θJC}	Thermal Resistance Junction to Case		4.2	

ELECTRICAL CHARACTERISTICS($T_A=25^\circ\text{C}$ Unless otherwise noted)

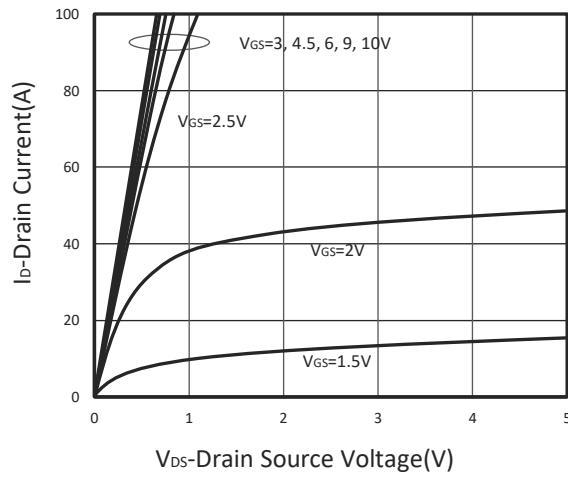
Symbol	Parameter	Condition	Min	Typ	Max	Unit	
Static Parameters							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	20			V	
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.4	0.6	1	V	
I_{GSS}	Gate Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			± 100	nA	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$		1		μA	
		$V_{DS}=16\text{V}$, $V_{GS}=0\text{V}$, $T_J=75^\circ\text{C}$		10			
$R_{DS(\text{ON})}$	Drain-source On-Resistance ^D	$V_{GS}=10\text{V}$, $I_D=20\text{A}$		2.7	3.5	$\text{m}\Omega$	
		$V_{GS}=4.5\text{V}$, $I_D=20\text{A}$		3.3	4.5		
		$V_{GS}=2.5\text{V}$, $I_D=10\text{A}$		4.2	5.5		
		$V_{GS}=1.8\text{V}$, $I_D=5\text{A}$		6.6	8.8		
G_f	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=10\text{A}$		33		S	
Diode Characteristics							
V_{SD}	Diode Forward Voltage ^D	$I_S=1\text{A}$, $V_{GS}=0\text{V}$			1	V	
I_S	Diode Continuous Forward Current [*]				50	A	
t_{rr}	Reverse Recovery Time			19		ns	
Q_{rr}	Reverse Recovery Charge	$I_S=10\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		9.2		nC	
Dynamic and Switching Parameters^E							
Q_g	Total Gate Charge	$V_{DS}=10\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=20\text{A}$		30	42		
Q_{gs}	Gate-Source Charge			5.1	7.1		
Q_{gd}	Gate-Drain Charge			10	14		
C_{iss}	Input Capacitance	$V_{DS}=10\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$		3520		pF	
C_{oss}	Output Capacitance			572			
C_{rss}	Reverse Transfer Capacitance			425			
R_g	Gate Resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $F=1\text{MHz}$		2.1		Ω	
$t_{d(on)}$	Turn-On Time	$V_{DD}=10\text{V}$, $V_{GS}=4.5\text{V}$ $R_G=3\Omega$, $I_D=1\text{A}$		12.7	24	nS	
t_r				15.2	29		
$t_{d(off)}$	Turn-Off Time			85	162		
t_f				37	70		

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

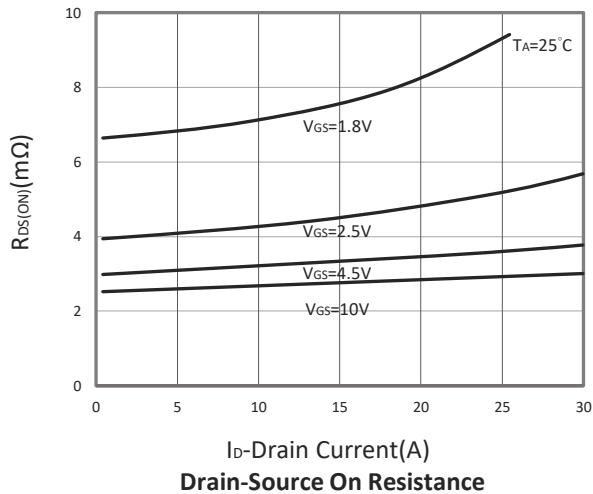
- A. Surface mounted on FR4 board using 1 in² pad size.
- B. Pulsed width limited by maximum junction temperature, $T_{J(\text{MAX})}=150^\circ\text{C}$.
- C. Using $\leq 10\text{s}$ junction-to-ambient thermal resistance is base on $T_{J(\text{MAX})}=150^\circ\text{C}$.
- D. Pulse test width $\leq 300\mu\text{s}$ and duty cycle $\leq 2\%$.
- E. Guaranteed by design, not subject to production testing.
- *. The maximum rating current is limited by bonding wire.

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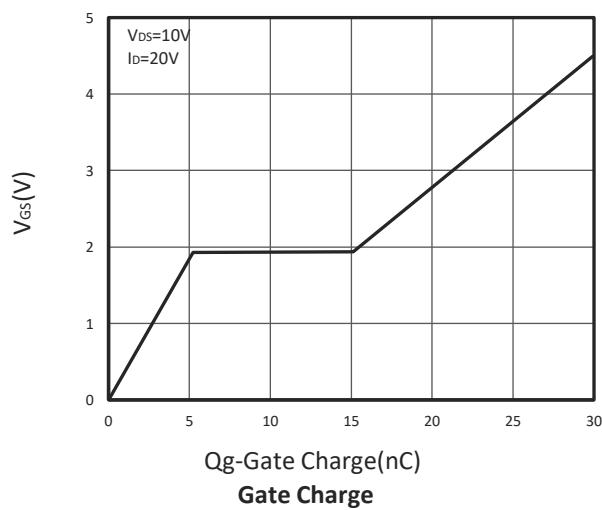
TYPICAL CHARACTERISTICS



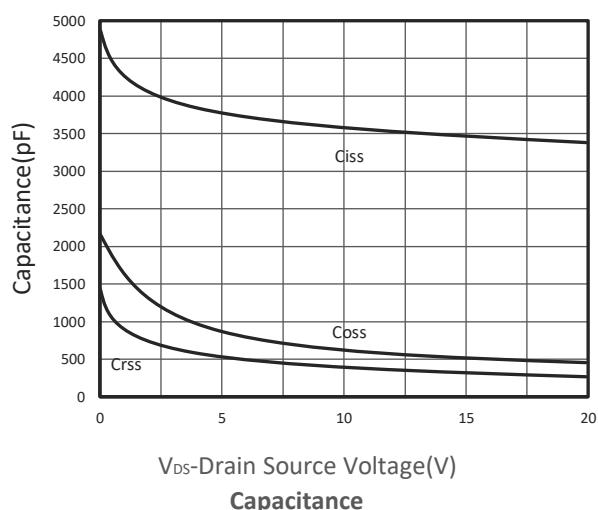
I_D -Drain Current(A)
 V_{DS} -Drain Source Voltage(V)
Output Characteristics



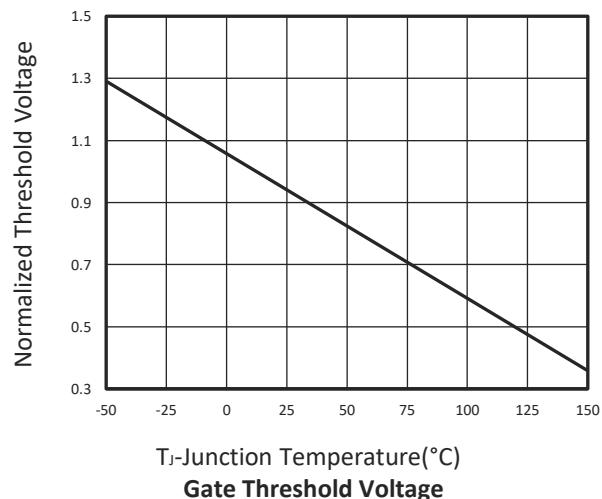
I_D -Drain Current(A)
 $R_{DS(on)}$ (mΩ)
Drain-Source On Resistance



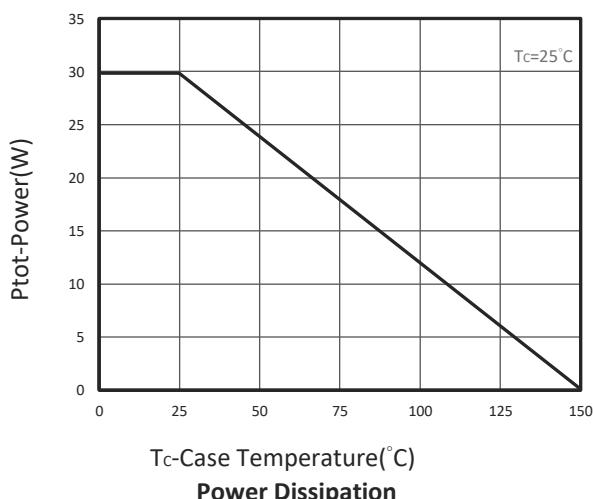
V_{GS} (V)
 Q_g -Gate Charge(nC)
Gate Charge



V_{DS} -Drain Source Voltage(V)
Capacitance

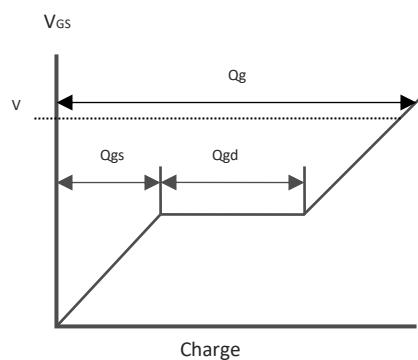
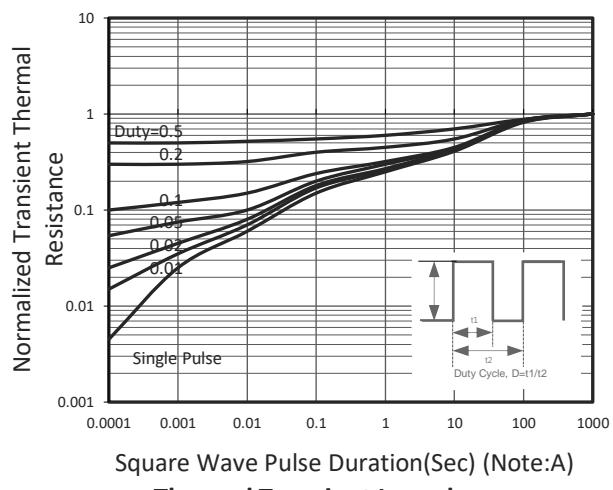
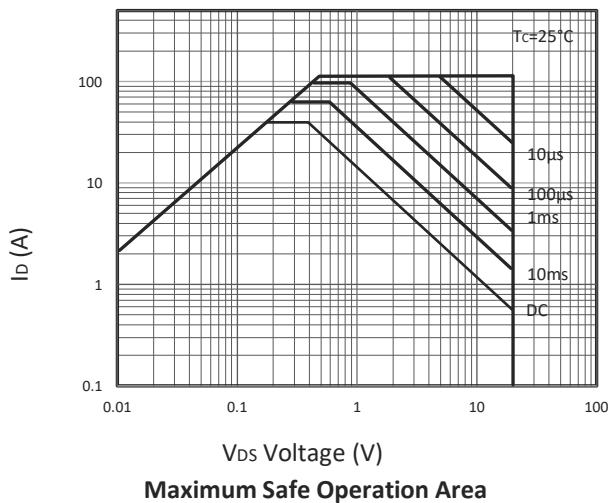
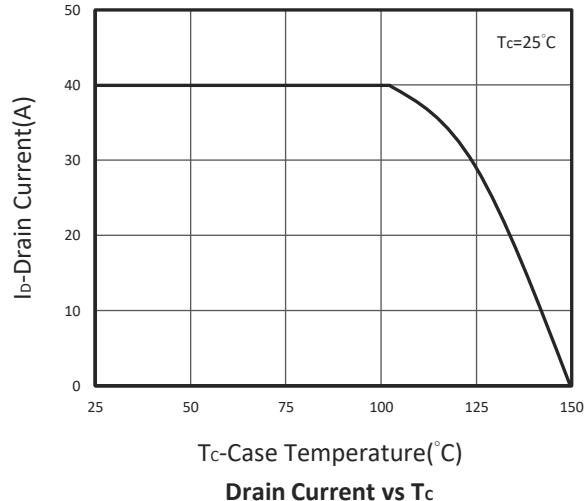
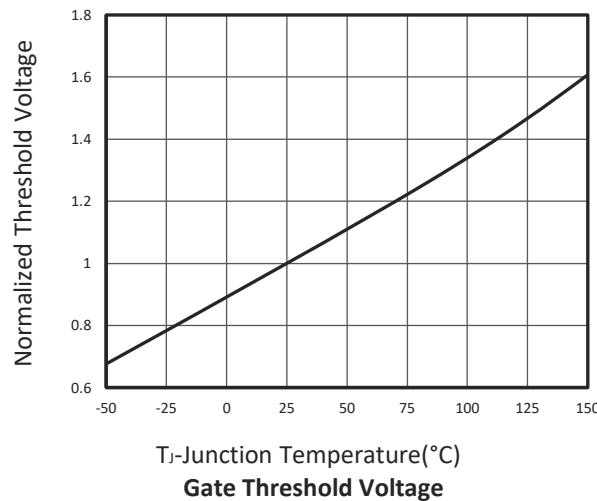


T_J -Junction Temperature(°C)
Gate Threshold Voltage

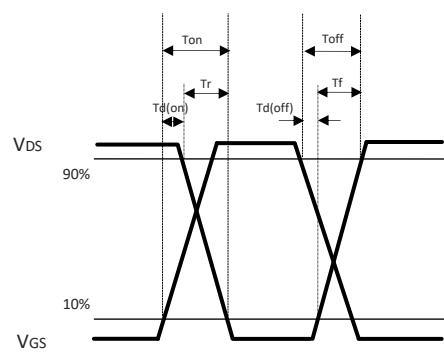


T_c -Case Temperature(°C)
Power Dissipation

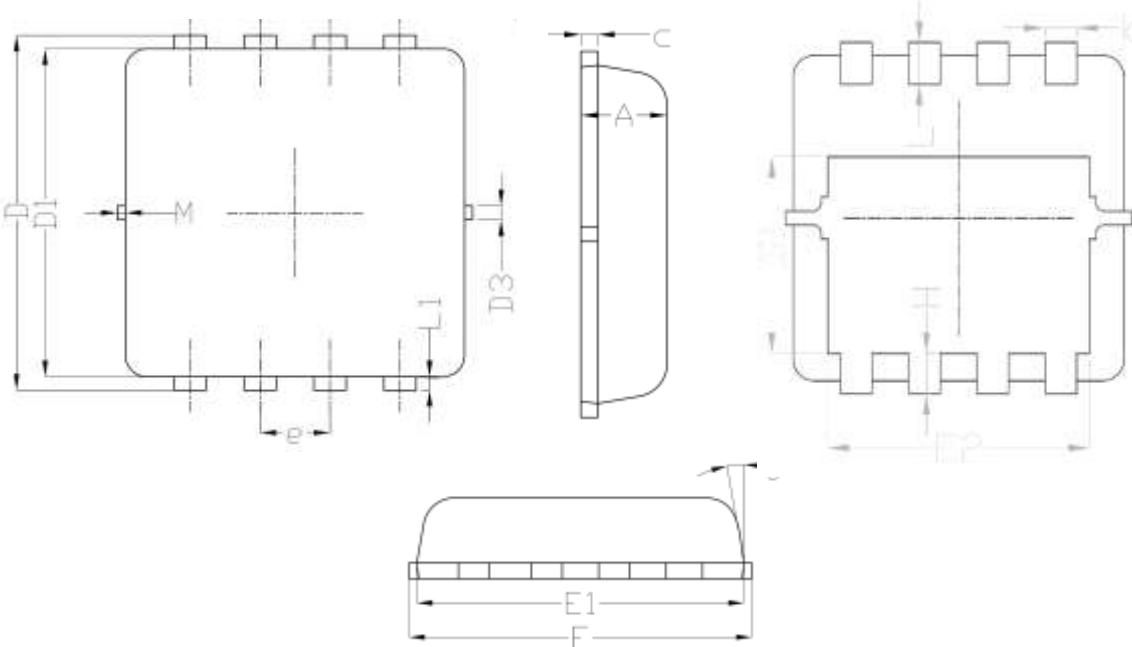
■ TYPICAL CHARACTERISTICS



Gate Charge Waveform



Switching Time Waveform

■ DFN3.3X3.3A-8 PACKAGE DIMENSIONS


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.014
c	0.100	0.250	0.004	0.010
D	3.250	3.450	0.128	0.136
D1	3.000	3.200	0.118	0.126
D2	1.780	1.980	0.070	0.078
D3	-	0.130	-	0.005
E	3.200	3.400	0.126	0.134
E1	3.000	3.200	0.118	0.126
E2	2.390	2.590	0.094	0.102
e	0.65BSC.		0.026BSC.	
H	0.300	0.500	0.012	0.020
L	0.300	0.500	0.012	0.020
L1	-	0.130	-	0.005
M	-	0.150	-	0.006
Θ	0°	12°	0°	12°

Recommended Land Pattern

