

Single P-Channel MOSFET

■ DESCRIPTION

STP9435M is the P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior fast switching performance. These devices are well suited for high efficiency fast switching applications.

■ PART NUMBER INFORMATION

SMC 9435 M - TR G

a	b	c	d	e
---	---	---	---	---

a : Company name.

b : Product Serial number.

c : Package code M:SOP-8

d : Handling code TR:Tape&Reel

e : Green produce code G:RoHS Compliant

■ FEATURES

$V_{DS}=-30V$, $I_D=-6.5A$

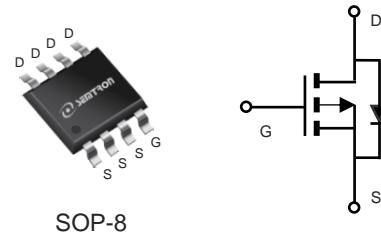
$R_{DS(ON)}=40m\Omega$ (Typ.) @ $V_{GS}=-10V$

$R_{DS(ON)}=54m\Omega$ (Typ.) @ $V_{GS}=-4.5V$

- ◆ Fast switch
- ◆ Low gate charge
- ◆ High power and current handling capability

■ APPLICATIONS

- ◆ Load Switch
- ◆ Portable Equipment
- ◆ DC-DC Power Management



■ ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_A=25^\circ C$ $T_A=70^\circ C$	-6.5 -5.2
I_{DM}	Pulsed Drain Current ^B	-26	A
I_{AS}	Avalanche Current ^B	-20	A
E_{AS}	Single Pulse Avalanche energy L=0.3mH ^B	60	mJ
P_D	Power Dissipation ^A	$T_A=25^\circ C$ $T_A=70^\circ C$	3.1 2
T_J	Operation Junction Temperature	-55/150	°C
T_{STG}	Storage Temperature Range	-55/150	°C

■ THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^A	$t \leq 10s$	40	°C/W
	Thermal Resistance Junction to Ambient ^{AC}	Steady-State	80	
$R_{\theta JC}$	Thermal Resistance Junction to Case		30	

ELECTRICAL CHARACTERISTICS($T_A=25^\circ\text{C}$ Unless otherwise noted)

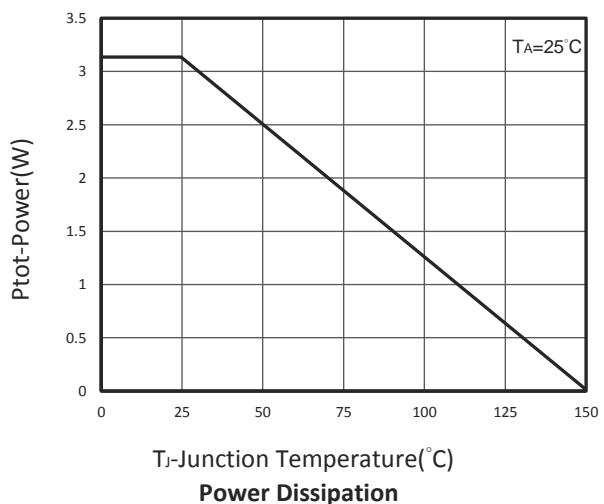
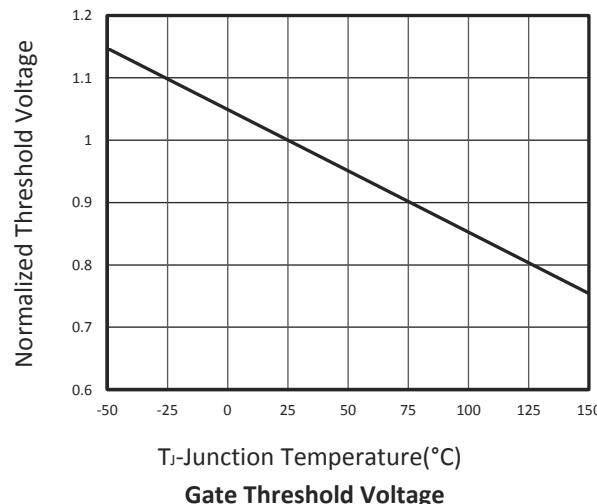
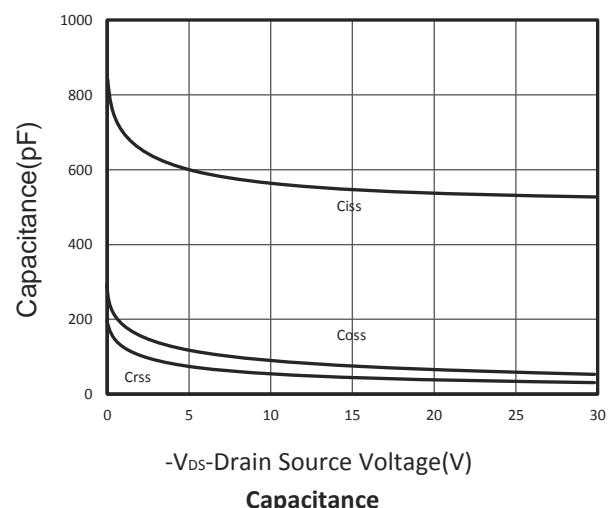
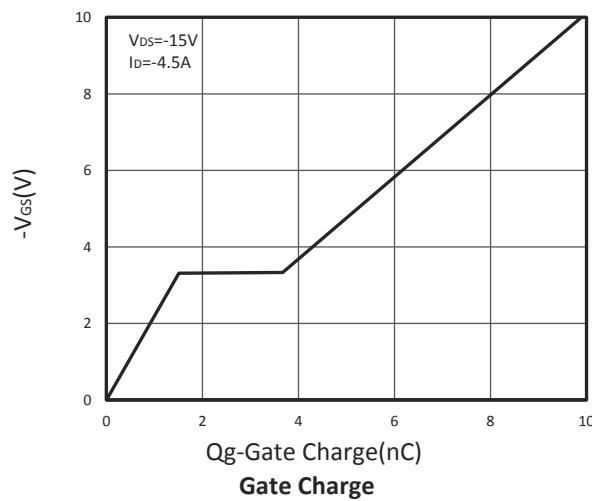
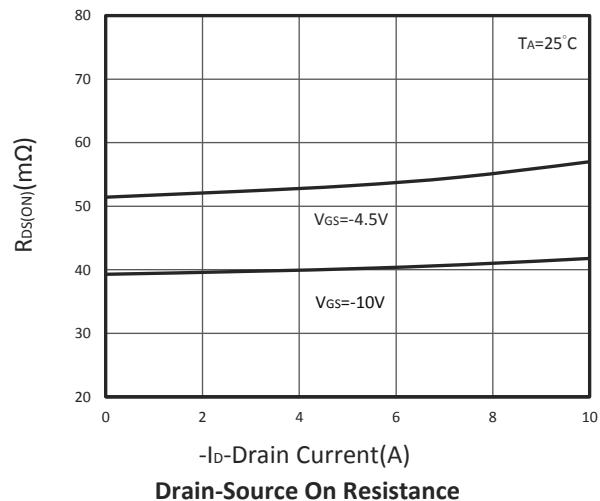
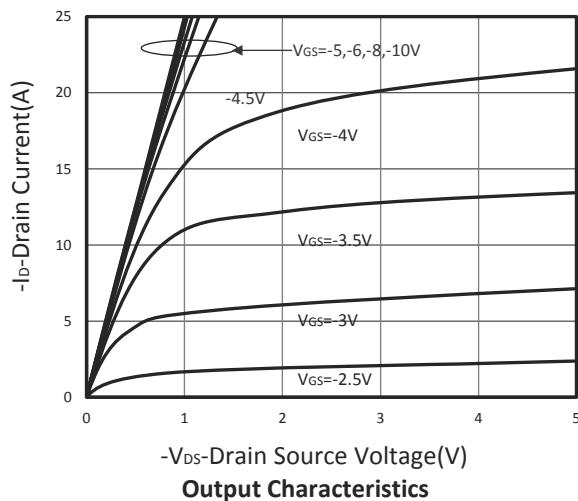
Symbol	Parameter	Condition	Min	Typ	Max	Unit	
Static Parameters							
BV_{DSS}	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=-250\mu\text{A}$	-30			V	
$\text{V}_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=-250\mu\text{A}$	-1	-1.5	-2	V	
I_{GSS}	Gate Leakage Current	$\text{V}_{\text{DS}}=0\text{V}, \text{V}_{\text{GS}}=\pm 20\text{V}$			± 100	nA	
I_{DSS}	Zero Gate Voltage Drain Current	$\text{V}_{\text{DS}}=-30\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{T}_J=25^\circ\text{C}$			-1	μA	
		$\text{V}_{\text{DS}}=-24\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{T}_J=75^\circ\text{C}$			-10		
$\text{R}_{\text{DS}(\text{ON})}$	Drain-source On-Resistance ^D	$\text{V}_{\text{GS}}=-10\text{V}, \text{I}_D=-6.5\text{A}$		40	48	$\text{m}\Omega$	
		$\text{V}_{\text{GS}}=-4.5\text{V}, \text{I}_D=-4\text{A}$		54	65		
G_{fs}	Forward Transconductance	$\text{V}_{\text{DS}}=-10\text{V}, \text{I}_D=-4.5\text{A}$		12		S	
Diode Characteristics							
V_{SD}	Diode Forward Voltage ^D	$\text{I}_S=-1\text{A}, \text{V}_{\text{GS}}=0\text{V}$			-1	V	
I_S	Diode Continuous Forward Current				-6.4	A	
t_{rr}	Revese Recovery Time	$\text{I}_S=-4.5\text{A}, \frac{d\text{I}}{dt}=100\text{A}/\mu\text{s}$		15		ns	
Q_{rr}	Revese Recovery Charg	$\text{T}_J=25^\circ\text{C}$		9.8		nC	
Dynamic and Switching Parameters^E							
Q_g	Total Gate Charge	$\text{V}_{\text{DS}}=-15\text{V}, \text{V}_{\text{GS}}=-10\text{V}$ $\text{I}_D=-4.5\text{A}$		9.8	13.8	nC	
Q_g	Total Gate Charge (4.5V)			4.8	6.7		
Q_{gs}	Gate-Source Charge			1.7	2.4		
Q_{gd}	Gate-Drain Charge			2	2.8		
C_{iss}	Input Capacitance	$\text{V}_{\text{DS}}=-15\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{f}=1\text{MHz}$		580		pF	
C_{oss}	Output Capacitance			68			
C_{rss}	Reverse Transfer Capacitance			58			
$\text{t}_{\text{d}(\text{on})}$	Turn-On Time ^D	$\text{V}_{\text{DD}}=-15\text{V}, \text{V}_{\text{GEN}}=-10\text{V}$ $\text{R}_G=6\Omega, \text{I}_D=-1\text{A}$		8.3		nS	
t_r				10			
$\text{t}_{\text{d}(\text{off})}$	Turn-Off Time ^D			16.8			
t_f				7.8			

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

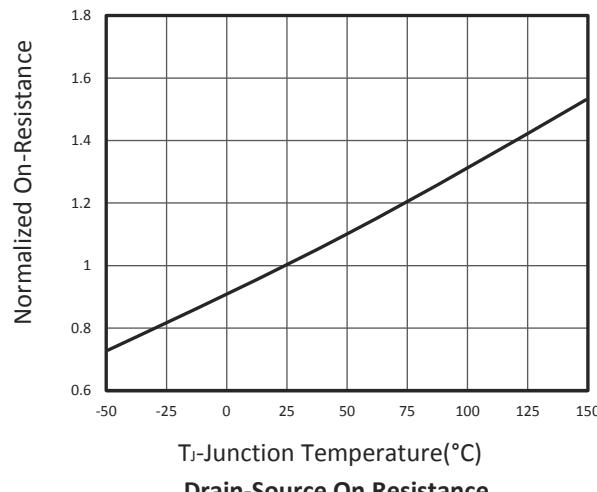
- A. Surface mounted on FR4 board using 1 in² pad size.
- B. Pulsed width limited by maximum junction temperature, $\text{T}_J(\text{MAX})=150^\circ\text{C}$ (initial temperature $\text{T}_J=25^\circ\text{C}$).
- C. Using $\leq 10\text{s}$ junction-to-ambient thermal resistance is base on $\text{T}_J(\text{MAX})=150^\circ\text{C}$.
- D. Pulse test width $\leq 300\mu\text{s}$ and duty cycle $\leq 2\%$.
- E. Guaranteed by design, not subject to production testing.

The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date. We assume no responsibility for any infringement of patents, patent rights, or other rights arising from the use of any information and circuitry in this datasheet.

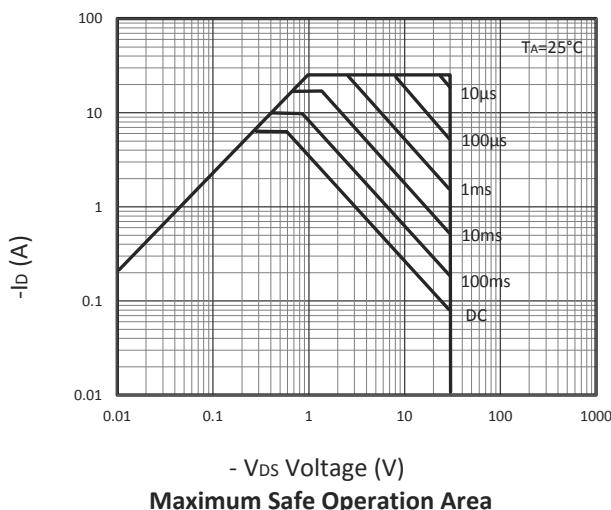
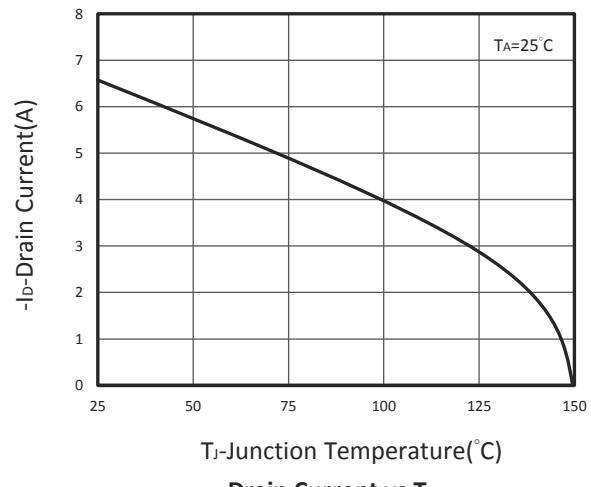
TYPICAL CHARACTERISTICS



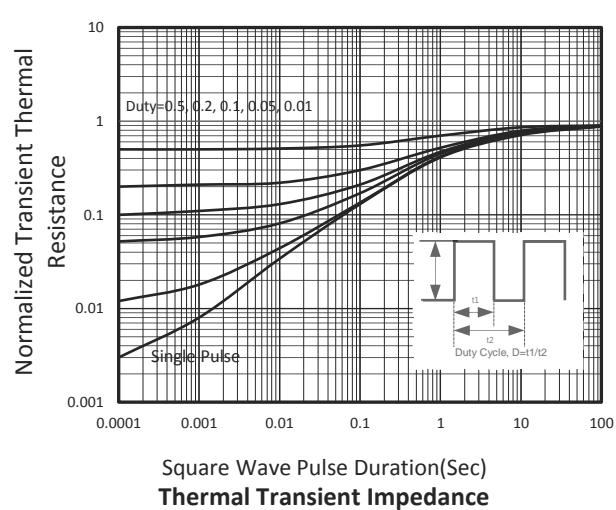
TYPICAL CHARACTERISTICS



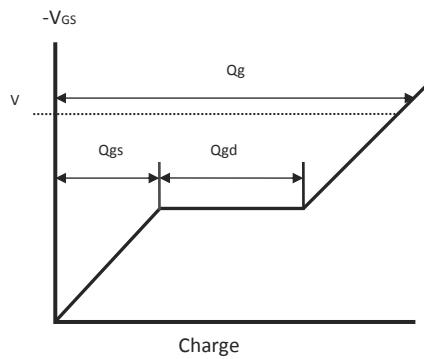
T_j -Junction Temperature(°C)
Drain Current vs T_j



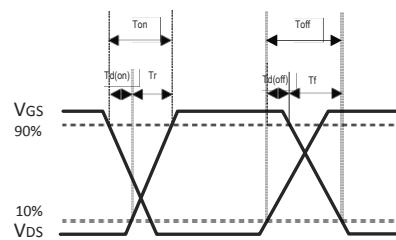
- V_{DS} Voltage (V)
Maximum Safe Operation Area



Square Wave Pulse Duration(Sec)
Thermal Transient Impedance

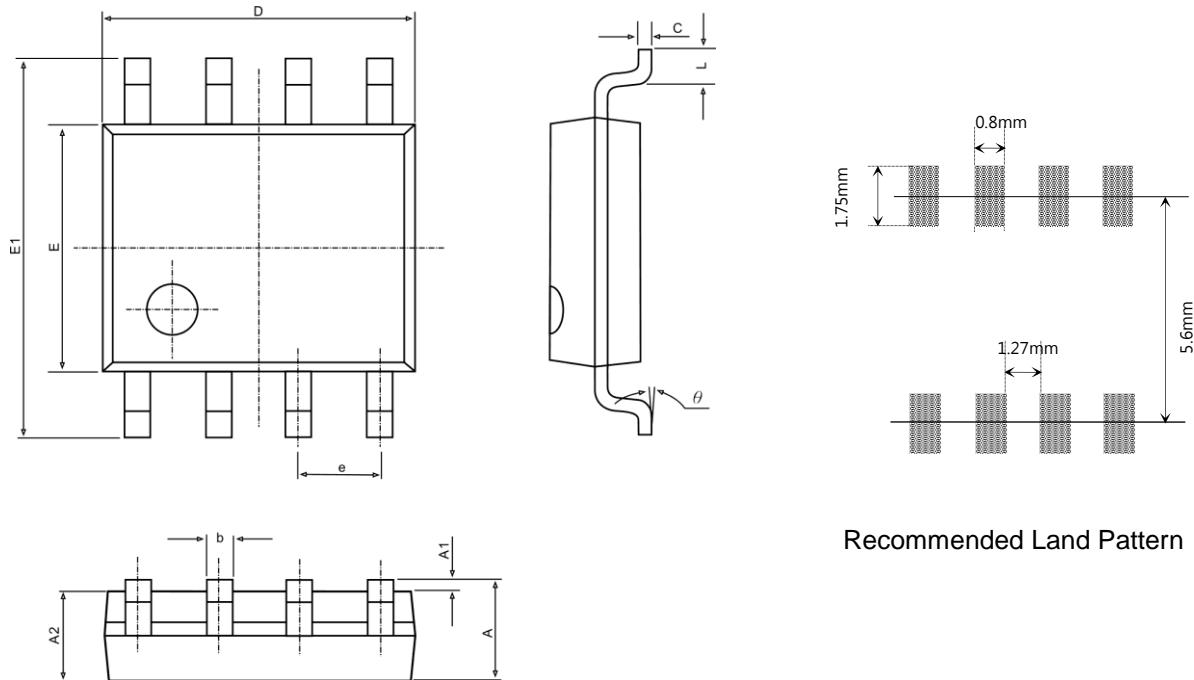


Gate Charge Waveform



Switching Time Waveform

SOP-8 PACKAGE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.040	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.130	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270BSC.		0.050BSC.	
L	0.400	1.270	0.016	0.005
Θ	0°	8°	0°	8°